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Serial No. 10/605,478

In The Claims:

Claim 1. (currently amended) A silicon oxide gap-filling process, comprising:
providing a substrate having a trench thereon, wherein an aspect ratio of the trench is 4.0 at least; and

performing a CVD process having an etching effect to fill up the trench with silicon oxide, wherein reaction gases used in the CVD process comprise deposition gases and He/H₂ mixed gas as a sputtering-etching gas, wherein an ED ratio of the CVD process is 0.03-0.1 and a percentage of the He/H₂ mixed gas in the total reaction gases is 70% at least.

Claim 2. (original) The silicon oxide gap-filling process of claim 1, wherein the CVD process comprises an HDP-CVD process.

Claim 3. (original) The silicon oxide gap-filling process of claim 1, wherein a ratio of He to H₂ (He/H₂ ratio) in the He/H₂ mixed gas is 0.3-4.0.

Claim 4. (Cancelled)

Claim 5. (original) The silicon oxide gap-filling process of claim 1, wherein the deposition gases comprise SiH₄ and O₂.

Claim 6. (original) The silicon oxide gap-filling process of claim 5, wherein in the CVD process, a flow rate of SiH₄ is 20-100sccm, a flow rate of O₂ is 40-200sccm, a flow rate of H₂ is 100-2000sccm, a flow rate of He is 200-2000sccm, a pressure is 5-20mTorr, a temperature is 400-650°C, a low-frequency RF power is 3000-15000W, and a high-frequency RF power is

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500-5000W.

Claim 7. (original) The silicon oxide gap-filling process of claim 1, which is applied to an STI process in a 90nm semiconductor process.

Claims 8-15. (Cancelled)

Claim 16. (Currently amended) A silicon oxide gap-filling process, comprising:

providing a substrate having a trench thereon, wherein an aspect ratio of the trench is at least 4.0;

performing an HDP-CVD process to fill up the trench with silicon oxide, wherein reaction gases used in the HDP-CVD process comprise SiH_4 , O_2 , He and H_2 , wherein a flow rate of SiH_4 is 20-100sccm, a flow rate of O_2 is 40-200sccm, a flow rate of H_2 is 100-2000sccm, a flow rate of He is 200-2000sccm, a pressure is 5-20mTorr, a temperature is 400-650°C, a low-frequency RF power is 3000-15000W, and a high-frequency RF power is 500-5000W;

an ED ratio of the HDP-CVD process is 0.1-0.03; and

a percentage of the He/H_2 mixed gas in the total reaction gases is at least 70%[[a percentage of the He/H_2 in the total reaction gases is raised with increase of an aspect ratio of the trench]].

Claims 17-19. (Cancelled)

Claim 20. (Currently amended) The silicon oxide gap-filling process of claim ~~[[19]]~~16, which is applied to an STI process in a 90nm semiconductor process.